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GLOBAL POSITIONING SYSTEMS DIRECTORATE
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INTERFACE SPECIFICATION
IS-GPS-200

NAVSTAR GPS Space Segment/Navigation User Segment Interfaces

AUTHENTICATED BY: ______________________ 19 JAN 17

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IS200-1286 : (Section 3.2.1.5.1)

WAS :

Table 3-Ib. Expanded Code Phase Assignments (III and subsequent blocks only)

SV ID No.	GPS PRN Signal No.	Code Phase Selection			P-code Relative Advance (Hours) **	First 10 Chips Octal* C/A	First 12 Chips Octal P
		G2 Delay (Chips)	Initial G2 Setting (Octal)*	X2 Delay (Chips)			
70	38	67	0017	1	P_1(t+24)	1760	3373
71	39	103	0541	2	P_2(t+24)	1236	3757
72	40	91	1714	3	P_3(t+24)	0063	7545
73	41	19	1151	4	P_4(t+24)	0626	5440
74	42	679	1651	5	P_5(t+24)	0126	4402
75	43	225	0103	6	P_6(t+24)	1674	4023
76	44	625	0543	7	P_7(t+24)	1234	0233
77	45	946	1506	8	P_8(t+24)	0271	2337
78	46	638	1065	9	P_9(t+24)	0712	3375
79	47	161	1564	10	P_{10}(t+24)	0213	3754
80	48	1001	1365	11	P_{11}(t+24)	0412	3544
81	49	554	1541	12	P_{12}(t+24)	0236	7440
82	50	280	1327	13	P_{13}(t-24)	0450	1402
83	51	710	1716	14	P_{14}(t+24)	0061	6423
84	52	709	1635	15	P_{15}(t+24)	0142	1033
85	53	775	1002	16	P_{16}(t+-24)	0775	2637
86	54	864	1015	17	P_{17}(t+24)	0762	7135
87	55	558	1666	18	P_{18}(t+24)	0111	5674
88	56	220	0177	19	P_{19}(t+24)	1600	0514
89	57	397	1353	20	P_{20}(t+24)	0424	6064
90	58	55	0426	21	P_{21}(t+24)	1351	1210
91	59	898	0227	22	P_{22}(t+24)	1550	6726
92	60	759	0506	23	P_{23}(t+24)	1271	1171
93	61	367	0336	24	P_{24}(t+24)	1441	6656
94	62	299	1333	25	P_{25}(t+24)	0444	1105
95	63	1018	1745	26	P_{26}(t+24)	0032	6660

*In the octal notation for the first 10 chips of the C/A-code or the initial settings as shown in this table, the first digit (1/0) represents a "1" or “0”, respectively, for the first chip and the last three digits are the conventional octal representation of the remaining 9 chips

(For example, the first 10 chips of the C/A code for PRN Signal Assembly No. 38 are: 1111110000).

** P_i(t+N): P-code sequence of PRN number i shifted by N hours. See Section 3.3.2.1.

NOTE #1: The code phase assignments constitute inseparable pairs, each consisting of a specific C/A and a specific P code phase, as shown above.

NOTE #2: PRNs 38-63 are required per this Table if a manufacturer chooses to include these PRNs in their receiver design.

IS :

Table 3-Ib. Expanded Code Phase Assignments (III and subsequent blocks only)

SV ID No.	GPS PRN Signal No.	Code Phase Selection: G2 Delay (Chips)	Code Phase Selection: Initial G2 Setting (Octal)*	Code Phase Selection: X2 Delay (Chips)	P-code Relative Advance (Hours) **	First 10 Chips Octal* C/A	First 12 Chips Octal P
70	38	67	0017	1	P_{1}(t+24)	1760	3373
71	39	103	0541	2	P_{2}(t+24)	1236	3757
72	40	91	1714	3	P_{3}(t+24)	0063	7545
73	41	19	1151	4	P_{4}(t+24)	0626	5440
74	42	679	1651	5	P_{5}(t+24)	0126	4402
75	43	225	0103	6	P_{6}(t+24)	1674	4023
76	44	625	0543	7	P_{7}(t+24)	1234	0233
77	45	946	1506	8	P_{8}(t+24)	0271	2337
78	46	638	1065	9	P_{9}(t+24)	0712	3375
79	47	161	1564	10	P_{10}(t+24)	0213	3754
80	48	1001	1365	11	P_{11}(t+24)	0412	3544
81	49	554	1541	12	P_{12}(t+24)	0236	7440
82	50	280	1327	13	P_{13}(t+24)	0450	1402
83	51	710	1716	14	P_{14}(t+24)	0061	6423
84	52	709	1635	15	P_{15}(t+24)	0142	1033
85	53	775	1002	16	P_{16}(t+24)	0775	2637
86	54	864	1015	17	P_{17}(t+24)	0762	7135
87	55	558	1666	18	P_{18}(t+24)	0111	5674
88	56	220	0177	19	P_{19}(t+24)	1600	0514
89	57	397	1353	20	P_{20}(t+24)	0424	6064
90	58	55	0426	21	P_{21}(t+24)	1351	1210
91	59	898	0227	22	P_{22}(t+24)	1550	6726
92	60	759	0506	23	P_{23}(t+24)	1271	1171
93	61	367	0336	24	P_{24}(t+24)	1441	6656
94	62	299	1333	25	P_{25}(t+24)	0444	1105
95	63	1018	1745	26	P_{26}(t+24)	0032	6660

*In the octal notation for the first 10 chips of the C/A-code or the initial settings as shown in this table, the first digit (1/0) represents a "1" or "0", respectively, for the first chip and the last three digits are the conventional octal representation of the remaining 9 chips

(For example, the first 10 chips of the C/A code for PRN Signal Assembly No. 38 are: 1111110000).

** P_i(t+N): P-code sequence of PRN number i shifted by N hours. See Section 3.3.2.1.

NOTE #1: The code phase assignments constitute inseparable pairs, each consisting of a specific C/A and a specific P code phase, as shown above.

NOTE #2: PRNs 38-63 are required per this Table if a manufacturer chooses to include these PRNs in their receiver design.

IS200-48 : (Section 3.2.3)

WAS :

During the initial period of Block IIR-M SVs operation, prior to Initial Operational Capability of L2 C signal, Block IIR-M may modulo-2 add the NAV data, D(t), to the L2 CM-code instead of CNAV data, DC(t). In such configuration, the data rate of D(t) may be 50 bps (i.e. without convolution encoding) or it may be 25 bps. The D(t) of 25 bps shall be convolutionally encoded resulting in 50 sps.

IS :

~~During the initial period of Block IIR-M SVs operation, prior to Initial Operational Capability of L2 C signal, Block IIR-M may modulo-2 add the NAV data, D(t), to the L2 CM-code instead of CNAV data, DC(t). In such configuration, the data rate of D(t) may be 50 bps (i.e. without convolution encoding) or it may be 25 bps. The D(t) of 25 bps shall be convolutionally encoded resulting in 50 sps.~~

IS200-97 : (Section 3.3.2)

WAS :
For PRN codes 1 through 37, the $P_i(t)$ pattern (P-code) is generated by the modulo-2 summation of two PRN codes, X1(t) and X2(t - iT), where T is the period of one P-code chip and equals $(1.023E7)^{-1}$ seconds, while i is an integer from 1 through 37. This allows the generation of 37 unique P(t) code phases (identified in Table 3-Ia) using the same basic code generator.

Expanded P-code PRN sequences, $P_i(t)$ where $38 \leq i \leq 63$, are described as follows:

$P_i(t) = P_{i-37}(t - T)$ where T will equal 24 hours)

therefore, the equation is

$P_i(t) = P_{i-37x}(t + i * 24 \text{ hours})$,

where i is an integer from 64 to 210, x is an integer portion of (i-1)/37.

As an example, the P-code sequence for PRN 38 is the same sequence as PRN 1 shifted 24 hours into a week (i.e. 1st chip of PRN 38 at beginning of week is the same chip for PRN 1 at 24 hours after beginning of week). The list of expanded P-code PRN assignments is identified in Table 3-Ib.

The linear $G_i(t)$ pattern (C/A-code) is the modulo-2 sum of two 1023-bit linear patterns, G1 and $G2_i$. The latter sequence is selectively delayed by an integer number of chips to produce many different G(t) patterns (defined in Tables 3-Ia and 3-Ib).

The $C_{M,i}(t)$ pattern (L2 CM-code) is a linear pattern which is reset with a specified initial state every code count of 10230 chips. Different initial states are used to generate different $C_{M,i}(t)$ patterns (defined in Tables 3-IIa and 3-IIb).

The $C_{L,i}(t)$ pattern (L2 CL-code) is also a linear pattern but with a longer reset period of 767250 chips. Different initial states are used to generate different $C_{L,i}(t)$ patterns (defined in Tables 3-IIa and 3-IIb).

For a given SV ID, two different initial states are used to generate different $C_{L,i}(t)$ and $C_{M,i}(t)$ patterns.

Section 6.3.6 provides a selected subset of additional P-, L2 CM-, L2 CL-, and the C/A-code sequences with assigned PRN numbers.

IS :

For PRN codes 1 through 37, the $P_i(t)$ pattern (P-code) is generated by the modulo-2 summation of two PRN codes, X1(t) and X2(t - iT), where T is the period of one P-code chip and equals $(1.023E7)^{-1}$ seconds, while i is an integer from 1 through 37. This allows the generation of 37 unique P(t) code phases (identified in Table 3-Ia) using the same basic code generator.

Expanded P-code PRN sequences, $P_i(t)$ where $38 \leq i \leq 63$, are described as follows:

$P_i(t) = P_{i-37}(t \mathbin{-} \underline{+}\ T)$ where T will equal 24 hours)

therefore, the equation is

$P_i(t) = P_{i-37x}(t + i * 24 \text{ hours})$,

where i is an integer from 64 to 210, x is an integer portion of (i-1)/37.

As an example, the P-code sequence for PRN 38 is the same sequence as PRN 1 shifted 24 hours into a week (i.e. 1st chip of PRN 38 at beginning of week is the same chip for PRN 1 at 24 hours after beginning of week). The list of expanded P-code PRN assignments is identified in Table 3-Ib.

The linear $G_i(t)$ pattern (C/A-code) is the modulo-2 sum of two 1023-bit linear patterns, G1 and $G2_i$. The latter sequence is selectively delayed by an integer number of chips to produce many different G(t) patterns (defined in Tables 3-Ia and 3-Ib).

The $C_{M,i}(t)$ pattern (L2 CM-code) is a linear pattern which is reset with a specified initial state every code count of 10230 chips. Different initial states are used to generate different $C_{M,i}(t)$ patterns (defined in Tables 3-IIa and 3-IIb).

The $C_{L,i}(t)$ pattern (L2 CL-code) is also a linear pattern but with a longer reset period of 767250 chips. Different initial states are used to generate different $C_{L,i}(t)$ patterns (defined in Tables 3-IIa and 3-IIb).

For a given SV ID, two different initial states are used to generate different $C_{L,i}(t)$ and $C_{M,i}(t)$ patterns.

Section 6.3.6 provides a selected subset of additional P-, L2 CM-, L2 CL-, and the C/A-code sequences with assigned PRN numbers.

IS200-106 : (Section 3.3.2.2)

WAS :
The state of each generator can be expressed as a code vector word which specifies the binary sequence constant of each register as follows: (a) the vector consists of the binary state of each stage of the register, (b) the stage 12 value appears at the left followed by the values of the remaining states in order of descending stage numbers, and (c) the shift direction is from lower to higher stage number with stage 12 providing the current output. This code vector convention represents the present output and 11 future outputs in sequence. Using this convention, at each X1 epoch, the X1A shift register is initialized to code vector 001001001000 and the X1B shift register is initialized to code vector 010101010100. The first chip of the X1A sequence and the first chip of the X1B sequence occur simultaneously in the first chip interval of any X1 period.

IS :
The state of each generator can be expressed as a code vector word which specifies the binary sequence constant of each register as follows: (a) the vector consists of the binary state of each stage of the register (Note that in the code vector convention, the output is on the left while in Figures 3-2 through 3-5 the output tap is on the right.), (b) the stage 12 value appears at the left followed by the values of the remaining states in order of descending stage numbers, and (c) the shift direction is from lower to higher stage number with stage 12 providing the current output. This code vector convention represents the present output and 11 future outputs in sequence. Using this convention, at each X1 epoch, the X1A shift register is initialized to code vector 001001001000 and the X1B shift register is initialized to code vector 010101010100. The first chip of the X1A sequence and the first chip of the X1B sequence occur simultaneously in the first chip interval of any X1 period.

IS200-117 : (Section 3.3.2.2)

WAS :
Figure 3-6 shows a functional P-code mechanization for the 37 unique $P_i(t)$ code phases, $1 \leq i \leq 37$. 37 unique P(t) code phases. Signal component timing for these original P(t) code phases is shown in Figure 3-7, while the end-of-week reset timing and the final code vector states are given in Tables 3-VI and 3-VII, respectively.

IS :
Figure 3-6 shows a functional P-code mechanization for the 37 unique $P_i(t)$ code phases, $1 \leq i \leq 37$. ~~37 unique P(t) code phases.~~ Signal component timing for these original P(t) code phases is shown in Figure 3-7, while the end-of-week reset timing and the final code vector states are given in Tables 3-VI and 3-VII, respectively.

IS200-118 :

WAS :

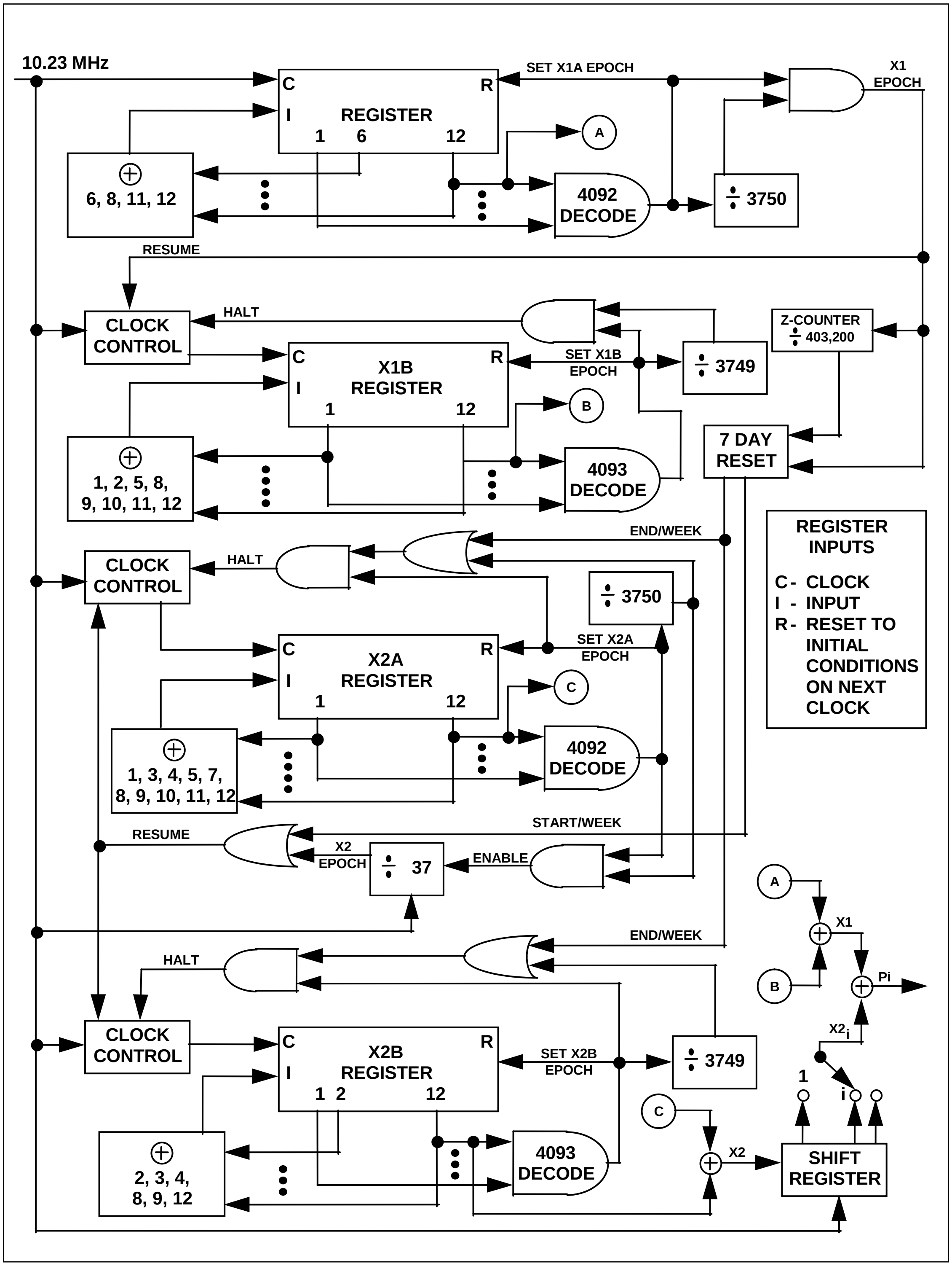

Figure 3-6. P-Code Generation

IS :

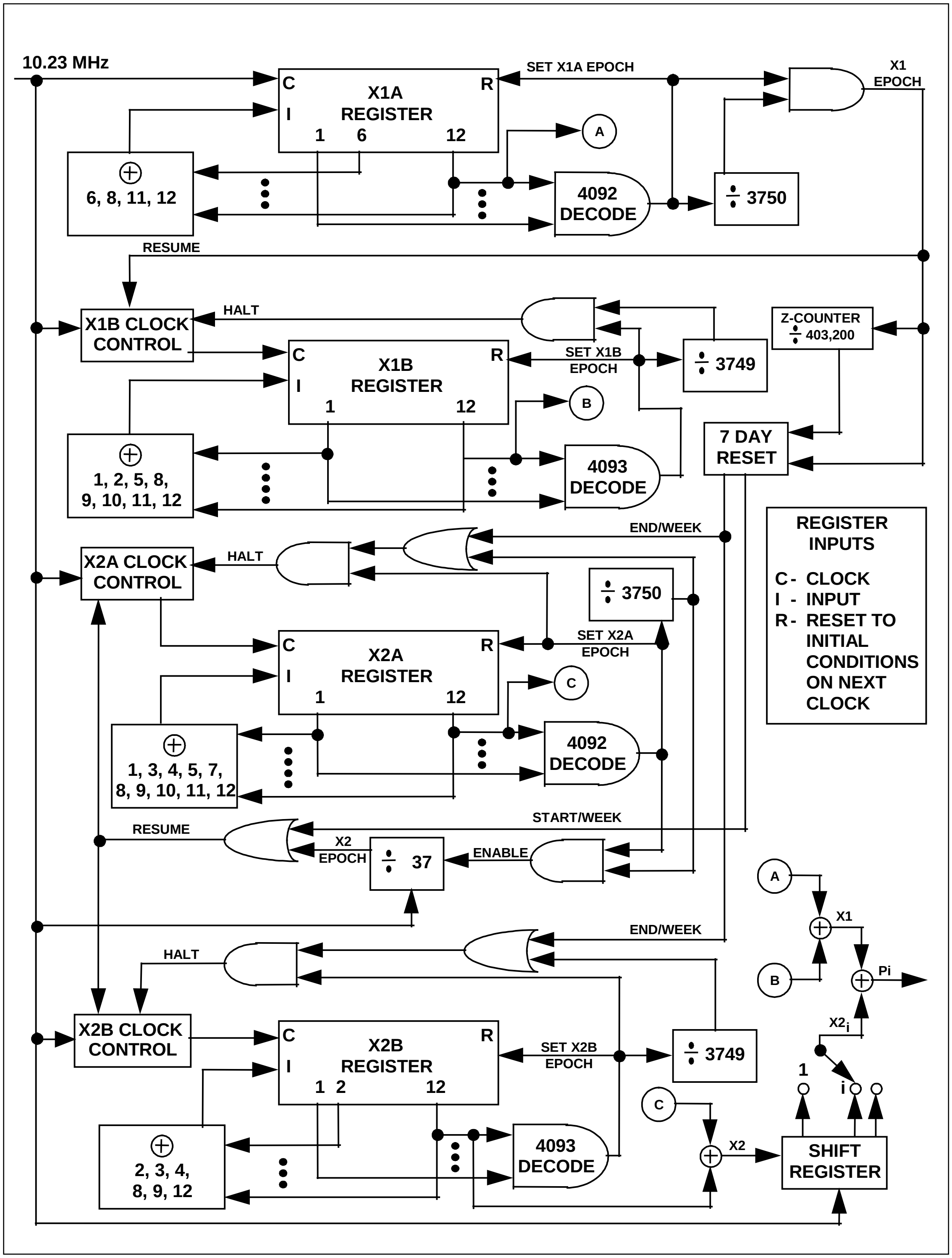

Figure 3-6. P-Code Generation

IS200-1511 : (Section 6.2.8)

WAS :
Invalid refers to a value that is within a data field's bit allocation and scale factor, but is outside the valid range and which GPS has no intention of functionally defining.

IS :
Invalid refers to a value that is within a data field's bit allocation and scale factor, but is outside the valid range and which GPS has no intention of functionally defining. Invalid range data is to be used at the user's own risk.

IS200-1282 : (Section 6.3.6.2)

WAS :

Table 6-I Additional C/A-/P-Code Phase Assignments (sheet 1 of 5)

PRN Signal No.	C/A			P		
	G2 Delay (Chips)	Initial G2 Setting (Octal)*	First 10 Chips (Octal)**	X2 Delay (Chips)	P-code Relative Advance (Hours) **	First 12 Chips (Octal)
64	729	0254	1523	27	P_{27}(t+24)	5112
65	695	1602	0175	28	P_{28}(t+24)	0667
66	780	1160	0617	29	P_{29}(t+24)	6111
67	801	1114	0663	30	P_{30}(t+24)	5266
68	788	1342	0435	31	P_{31}(t+24)	4711
69	732	0025	1752	32	P_{32}(t+24)	0166
70	34	1523	0254	33	P_{33}(t+24)	6251
71	320	1046	0731	34	P_{34}(t+24)	5306
72	327	0404	1373	35	P_{35}(t+24)	0761
73	389	1445	0332	36	P_{36}(t+24)	6152
74	407	1054	0723	37	P_{37}(t+24)	1247
75	525	0072	1705	1	P_{1}(t+48)	1736
76	405	0262	1515	2	P_{2}(t+48)	2575
77	221	0077	1700	3	P_{3}(t+48)	3054
78	761	0521	1256	4	P_{4}(t+48)	3604
79	260	1400	0377	5	P_{5}(t+48)	7520
80	326	1010	0767	6	P_{6}(t+48)	5472
81	955	1441	0336	7	P_{7}(t+48)	0417
82	653	0365	1412	8	P_{8}(t+48)	2025
83	699	0270	1507	9	P_{9}(t+48)	7230
84	422	0263	1514	10	P_{10}(t+48)	5736
85	188	0613	1164	11	P_{11}(t+48)	0575
86	438	0277	1500	12	P_{12}(t+48)	2054
87	959	1562	0215	13	P_{13}(t-48)	3204
88	539	1674	0103	14	P_{14}(t+48)	7720
89	879	1113	0664	15	P_{15}(t+48)	5572
90	677	1245	0532	16	P_{16}(t+48)	4457
91	586	0606	1171	17	P_{17}(t+48)	0005
92	153	0136	1641	18	P_{18}(t+48)	2220
93	792	0256	1521	19	P_{19}(t+48)	3332
94	814	1550	0227	20	P_{20}(t+48)	3777
95	446	1234	0543	21	P_{21}(t+48)	3555

* In the octal notation for the first 10 chips of the C/A-code or the initial settings as shown in this table, the first digit (1/0) represents a "1" or “0”, respectively, for the first chip and the last three digits are the conventional octal representation of the remaining 9 chips. (For example, the first 10 chips of the C/A code for PRN Signal Assembly No. 64 are: 1101010011).

** P_i(t+N): P-code sequence of PRN number i shifted by N hours. See Section 6.3.6.2.1.

NOTE: The code phase assignments constitute inseparable pairs, each consisting of a specific C/A and a specific P code phase, as shown above.

Table 6-I Additional C/A-/P-Code Phase Assignments (sheet 1 of 5)

PRN Signal No.	C/A			P		
	G2 Delay (Chips)	Initial G2 Setting (Octal)*	First 10 Chips (Octal)**	X2 Delay (Chips)	P-code Relative Advance (Hours) **	First 12 Chips (Octal)
64	729	0254	1523	27	P_{27}(t+24)	5112
65	695	1602	0175	28	P_{28}(t+24)	0667
66	780	1160	0617	29	P_{29}(t+24)	6111
67	801	1114	0663	30	P_{30}(t+24)	5266
68	788	1342	0435	31	P_{31}(t+24)	4711
69	732	0025	1752	32	P_{32}(t+24)	0166
70	34	1523	0254	33	P_{33}(t+24)	6251
71	320	1046	0731	34	P_{34}(t+24)	5306
72	327	0404	1373	35	P_{35}(t+24)	0761
73	389	1445	0332	36	P_{36}(t+24)	6152
74	407	1054	0723	37	P_{37}(t+24)	1247
75	525	0072	1705	1	P_{1}(t+48)	1736
76	405	0262	1515	2	P_{2}(t+48)	2575
77	221	0077	1700	3	P_{3}(t+48)	3054
78	761	0521	1256	4	P_{4}(t+48)	3604
79	260	1400	0377	5	P_{5}(t+48)	7520
80	326	1010	0767	6	P_{6}(t+48)	5472
81	955	1441	0336	7	P_{7}(t+48)	0417
82	653	0365	1412	8	P_{8}(t+48)	2025
83	699	0270	1507	9	P_{9}(t+48)	7230
84	422	0263	1514	10	P_{10}(t+48)	5736
85	188	0613	1164	11	P_{11}(t+48)	0575
86	438	0277	1500	12	P_{12}(t+48)	2054
87	959	1562	0215	13	P_{13}(t+48)	3204
88	539	1674	0103	14	P_{14}(t+48)	7720
89	879	1113	0664	15	P_{15}(t+48)	5572
90	677	1245	0532	16	P_{16}(t+48)	4457
91	586	0606	1171	17	P_{17}(t+48)	0005
92	153	0136	1641	18	P_{18}(t+48)	2220
93	792	0256	1521	19	P_{19}(t+48)	3332
94	814	1550	0227	20	P_{20}(t+48)	3777
95	446	1234	0543	21	P_{21}(t+48)	3555

* In the octal notation for the first 10 chips of the C/A-code or the initial settings as shown in this table, the first digit (1/0) represents a "1" or “0”, respectively, for the first chip and the last three digits are the conventional octal representation of the remaining 9 chips. (For example, the first 10 chips of the C/A code for PRN Signal Assembly No. 64 are: 1101010011).

** P_i(t+N): P-code sequence of PRN number i shifted by N hours. See Section 6.3.6.2.1.

NOTE: The code phase assignments constitute inseparable pairs, each consisting of a specific C/A and a specific P code phase, as shown above.

IS200-397 : (Section 20.3.3.5.1.2)

WAS :

Table 20-VI. Almanac Parameters

Parameter	No. of Bits**	Scale Factor (LSB)	Valid Range***	Units
e	16	2^{-21}	0.0 to 0.03	dimensionless
t_{oa}	8	2^{12}	0 to 602,112	seconds
δ_i****	16*	2^{-19}		semi-circles
$\dot{\Omega}$	16*	2^{-38}	-6.33E-07 to 0	semi-circles/sec
$\sqrt{A}$	24	2^{-11}	2530 to 8192	$\sqrt{\text{meters}}$
Ω_0	24*	2^{-23}		semi-circles
ω	24*	2^{-23}		semi-circles
M_0	24*	2^{-23}		semi-circles
a_{f0}	11*	2^{-20}		seconds
a_{f1}	11*	2^{-38}		sec/sec

* Parameters so indicated shall be two's complement with the sign bit (+ or -) occupying the MSB;

** See Figure 20-1 for complete bit allocation in subframe;

*** Unless otherwise indicated in this column, valid range is the maximum range attainable with indicated bit allocation and scale factor;

**** Relative to i_0 = 0.30 semi-circles.

IS :

Table 20-VI. Almanac Parameters				
Parameter	No. of Bits**	Scale Factor (LSB)	Valid Range***	Units
e	16	2^{-21}	0.0 to 0.03	dimensionless
t_{oa}	8	2^{12}	0 to 602,112	seconds
δ_i****	16*	2^{-19}		semi-circles
$\dot{\Omega}$	16*	2^{-38}	-1.19E-07 to 0	semi-circles/sec
$\sqrt{A}$	24	2^{-11}	2530 to 8192	$\sqrt{\text{meters}}$
Ω_0	24*	2^{-23}		semi-circles
ω	24*	2^{-23}		semi-circles
M_0	24*	2^{-23}		semi-circles
a_{f0}	11*	2^{-20}		seconds
a_{f1}	11*	2^{-38}		sec/sec

* Parameters so indicated shall be two's complement with the sign bit (+ or -) occupying the MSB;

** See Figure 20-1 for complete bit allocation in subframe;

*** Unless otherwise indicated in this column, valid range is the maximum range attainable with indicated bit allocation and scale factor;

**** Relative to i_0 = 0.30 semi-circles.

IS200-1491 : (Section 30.3.3.4.6.1)

WAS :

A 6-bit value of "000000" in the PRN_a field shall indicate that no further Status Words are contained in the remainder of the data block. In this event, all subsequent bits in the data block field shall be filler bits, i.e., alternating ones and zeros beginning with one.

IS :

A 6-bit value of "000000" in the PRN_a field shall indicate that ~~no further Status~~there ~~Words~~is ~~are~~no ~~contained~~data in the ~~remainder of the~~ reduced ~~data~~almanac ~~block~~packet. In this event, all subsequent bits through the last bit of the last packet in the ~~data~~message ~~block~~(bit ~~field~~272 for MT 31, bit 276 for MT 12) shall be filler bits, i.e., alternating ones and zeros beginning with one.

IS200-610 : (Section 30.3.3.4.6.2.1)

WAS :

Table 30-V. Midi Almanac Parameters

Parameter	No. of Bits**	Scale Factor (LSB)	Valid Range***	Units
t_{oa}	8	2^{12}	0 to 602,112	seconds
e	11	2^{-16}	0.0 to 0.03	dimensionless
δ_i****	11*	2^{-14}		semi-circles
$\dot{\Omega}$	11*	2^{-33}	-6.33E-07 to 0	semi-circles/sec
$\sqrt{A}$	17	2^{-4}	2530 to 8192	$\sqrt{\text{meters}}$
Ω_0	16*	2^{-15}		semi-circles
ω	16*	2^{-15}		semi-circles
M_0	16*	2^{-15}		semi-circles
a_{f0}	11*	2^{-20}		seconds
a_{f1}	10*	2^{-37}		sec/sec

* Parameters so indicated shall be two's complement with the sign bit (+ or -) occupying the MSB;

** See Figure 30-10 for complete bit allocation in message type 37;

*** Unless otherwise indicated in this column, valid range is the maximum range attainable with indicated bit allocation and scale factor;

**** Relative to i_0 = 0.30 semi-circles.

IS :

Table 30-V. Midi Almanac Parameters				
Parameter	No. of Bits**	Scale Factor (LSB)	Valid Range***	Units
t_{oa}	8	2^{12}	0 to 602,112	seconds
e	11	2^{-16}	0.0 to 0.03	dimensionless
δ_i****	11*	2^{-14}		semi-circles
$\dot{\Omega}$	11*	2^{-33}	-1.19E-07 to 0	semi-circles/sec
$\sqrt{A}$	17	2^{-4}	2530 to 8192	$\sqrt{\text{meters}}$
Ω_0	16*	2^{-15}		semi-circles
ω	16*	2^{-15}		semi-circles
M_0	16*	2^{-15}		semi-circles
a_{f0}	11*	2^{-20}		seconds
a_{f1}	10*	2^{-37}		sec/sec

* Parameters so indicated shall be two's complement with the sign bit (+ or -) occupying the MSB;

** See Figure 30-10 for complete bit allocation in message type 37;

*** Unless otherwise indicated in this column, valid range is the maximum range attainable with indicated bit allocation and scale factor;

**** Relative to i_0 = 0.30 semi-circles.